UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,719	12/29/2000	Dennis M. Briddell	062891.0463	8327

7590 06/16/2004

Baker Botts L.L.P.
2001 Ross Avenue
Dallas, TX 75201-2980

EXAMINER	
JONES, PRENELL P	

ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,719	BRIDDELL ET AL.	
	Examiner	Art Unit	
	Prenell P Jones	2667	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 10, 13-20* is/are rejected.

7)☐ Claim(s) *7-9,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-5 and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sheikh et al in view of Garcen et al.

Regarding claims 1, 2, 4, 13, 14, 17, 18 and 20, Sheikh discloses (Abstract, Figs. 1-3, col. 3, line 18 thru col. 5, line 67) managing communications among computer devices (plurality modules) wherein the architecture include a fabric controller managing

communication between peer and host devices, fabric controller managing the flow of transaction request, a main host bus, other buses to support communication among peripheral devices, a common bus known in the art which is a PCI bus that supports communication by PCI devices to host and other devices, form of transaction depends of bus protocol, plurality of PCI devices, plurality of peer devices and host communicating via plurality I/O buses. Sheikh is silent of switching fabric for interfacing a host and multiple network modules/devices. In analogous art, Garcen discloses (Abstract, Fig1, col. 1, line 49 thru col. 7, line 15) monitoring/maintaining a plurality of modules wherein the plurality of modules communicate between switching modules which are associated with a switching fabric, whereby the switching modules consist of link controllers, communication between host processors and plurality of modules is implemented via switch modules/switch fabric, communication via PCI bus. In addition, it is inherent that buses are interfaces for communicating data/information/transactions. Therefore, it would have been obvious to one of ordinary skill in the art to implement a switching fabric for interfacing host/hosts and multiple communication devices/modules as taught by Garcen with the teachings of Sheikh to further provide additional control and managing/monitoring/maintaining of a system/network.

Regarding claims 3, 5, 15-16 and 19 as indicated above, Sheikh discloses (Abstract, Figs. 1-3, col. 3, line 18 thru col. 5, line 67) managing communications among computer devices (plurality modules) wherein the architecture include a fabric controller managing communication between peer and host devices, fabric controller managing the flow of

transaction request, a main host bus, other buses to support communication among peripheral devices, a common bus known in the art which is a PCI bus that supports communication by PCI devices to host and other devices, form of transaction depends of bus protocol, plurality of PCI devices, plurality of peer devices and host communicating via plurality I/O buses. Sheikh further discloses (col. 4, line 1-55) fabric PCI bridges for providing protocol conversion to connect PCI buses to other various protocol buses.

4. Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sheikh et al in view of Garcen et al as applied to claims 1-5 and 13-20 above, and further in view of Wooten et al.

Regarding claims 6, Sheikh discloses (Abstract, Figs. 1-3, col. 3, line 18 thru col. 5, line 67) managing communications among computer devices (plurality modules) wherein the architecture include a fabric controller managing communication between peer and host devices, fabric controller managing the flow of transaction request, a main host bus, other buses to support communication among peripheral devices, a common bus known in the art which is a PCI bus that supports communication by PCI devices to host and other devices, form of transaction depends of bus protocol, plurality of PCI devices, plurality of peer devices and host communicating via plurality I/O buses, and Garcen discloses (Abstract, Fig1, col. 1, line 49 thru col. 7, line 15) monitoring/maintaining a plurality of modules wherein the plurality of modules communicate between switching

modules which are associated with a switching fabric, whereby the switching modules consist of link controllers, communication between host processors and plurality of modules is implemented via switch modules/switch fabric, communication via PCI bus. In addition, it is inherent that buses are interfaces for communicating data/information/transactions. However, Sheikh and Garcen are silent on bus controller associated with a host bus/peer bus. In analogous art, Wooten discloses (Abstract, col. 2, line 15-67, col. 4, line 41 thru col. 5, line 23, col. 17, line 37-65) a communication system that manages the sending/receiving of data information between nodes/modules wherein the architecture consist of multiple I/O devices (plurality modules) wherein messages and commands are transferred between devices via buses such as host processor buses, bus controllers for controlling communication among devices such as peer/host devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement bus controllers associated with host/peer devices as taught by Wooten with the combined teachings of Sheikh and Garcen for the purpose of linking various buses for communication requirements.

Regarding claim 10, as indicated above, Wooten discloses (Abstract, col. 2, line 15-67, col. 4, line 41 thru col. 5, line 23, col. 17, line 37-65) a communication system that manages the sending/receiving of data information between nodes/modules wherein the architecture consist of multiple I/O devices (plurality modules) wherein messages and commands are transferred between devices via buses such as host processor buses, bus controllers for controlling communication among devices such as peer/host devices.

Wooten further discloses (Abstract, col. 17, line 37-67) upstream/downstream devices wherein the clock frequencies maybe different.

Allowable Subject Matter

5. Claims 7, 8, 9, 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although the combined cited art of Sheikh managing communications among computer devices (plurality modules) wherein the architecture include a fabric controller managing communication between peer and host devices, fabric controller managing the flow of transaction request, a main host bus, other buses to support communication among peripheral devices, a common bus known in the art which is a PCI bus that supports communication by PCI devices to host and other devices, form of transaction depends of bus protocol, plurality of PCI devices, plurality of peer devices and host communicating via plurality I/O buses, Garcen discloses monitoring/maintaining a plurality of modules wherein the plurality of modules communicate between switching modules which are associated with a switching fabric, whereby the switching modules consist of link controllers, communication between host processors and plurality of modules is implemented via switch modules/switch fabric, communication via PCI bus, write posting buffers, upstream and downstream devices having different clock frequencies. In addition, it is inherent that buses are interfaces for communicating

data/information/transactions they fail to teach/suggest each network module interface consisting of a network module delayed read buffer, host delayed buffer and a processor initiator write buffer receiving information over host bus, peer bus carries layer two traffic, host bus carries layer three traffic and a clock driving the host bus and peer bus is derived from a clock driving the host communication link.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prenell P. Jones whose telephone number is 703-305-0630. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 703-305-4378. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prenell P. Jones

May 25, 2004

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 5/25/04